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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,596	06/23/2005	Nobuji Negishi	JP 020031	9077

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
ELAMIN, ABDELMONIEM I	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/540,596	NEGISHI ET AL.	
	Examiner	Art Unit	
	Abdelmoniem Elamin	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao, EU. Patent No. 0524712 A2 (cited by Applicant).

3. Claim 1, Nakao teaches circuit device comprising:

a first delay circuit for outputting data in response to a pulse of a clock signal [*31 of Fig. 4*]; and

a signal processing circuit for processing said outputted data from said first delay circuit, a signal processing circuit comprising a second delay circuit for outputting data in response to said pulse of said clock signal [*FF 32 of Fig. 4*],

wherein said circuit device comprises a control circuit [*XOR 62, NAND 52 of Fig. 4*] for controlling whether said second delay circuit should be supplied with said pulse of said clock signal on the basis of whether outputted data from said first delay circuit in response to said pulse of said clock signal is equal to data to be outputted from said first delay circuit in response to the next pulse [*see Fig. 5 and related discussion , also see col. 4, lines 38*].

4. Claim 2, Nakao teaches said signal processing circuit comprises a plurality of said second delay circuits, and wherein at least two second delay circuits of said plurality of second delay circuits are cascaded [*see Fig. 5*].

5. Claim 3, Nakao teaches each of said at least two second delay circuits comprises a plurality of data inputting portions for receiving data [*input D of Fig. 4*] and a plurality of data outputting portions for outputting data [*output Q of FF, Fig. 4*].

6. Claim 4, Nakao teaches said signal processing circuit comprises a plurality of said second delay circuits [*FF 32-34*], and wherein said signal processing circuit further comprises a logic circuit having an inputting portion for receiving outputted data from one second delay circuit of said plurality of second delay circuits and an outputting portion for outputting data to another second delay circuit of said plurality of second delay circuits [*seethe input D and output Q of Fig. 4*].

7. Claim 5, Nakao teaches said one second delay circuit has a plurality of data outputting portions, wherein said another second delay circuit has a plurality of data inputting portions, and wherein said logic circuit has a plurality of inputting portions for receiving outputted data from said plurality of data outputting portions of said one second delay circuit and a plurality of outputting potions for outputting data to said plurality of data inputting portions of said another second delay circuit.

8. Claim 6, Nakao teaches said control circuit comprises: a deciding circuit for deciding whether said second delay circuit should be supplied with said pulse of said clock signal on the basis of whether said outputted data from said first delay circuit in response to said pulse of said clock signal is equal to said data to be outputted from said first delay circuit in response to the next pulse [*XOR 62 of Fig. 4*]; and a clock driver for allowing or blocking supply of said pulse of said clock signal to said second delay circuit in accordance with a decision of said deciding circuit [*NAND 52 of Fig. 4*].

9. Claim 9, Nakao teaches each of said first delay circuits and second delay circuits is constructed by one or more D flip-flops [*D flip-flops 31*-34 of Fig. 4].

Allowable Subject Matter

10. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdelmoniem Elamin whose telephone number is 571-2727-3674. The examiner can normally be reached on MON - THUR 10:00 AM - 6::00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abdelmoniem Elamin
Primary Examiner
Art Unit 2116

August 20, 2006